



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|-----------------|-------------|----------------------|---------------------|------------------|
| 09/581,464 | 08/04/2000 | MARTIN SEIFERT | 301/49887 | 1341 |

21874 7590 10/22/2003
EDWARDS & ANGELL, LLP
P.O. BOX 9169
BOSTON, MA 02209

EXAMINER

LY, ANH VU H

| ART UNIT | PAPER NUMBER |
|----------|--------------|
|----------|--------------|

2667

9

DATE MAILED: 10/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/581,464

Applicant(s)

SEIFERT ET AL.

Examiner

Anh-Vu H Ly

Art Unit

2667

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 19-36 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☐ Claim(s) 19-33 and 36 is/are rejected.
- 7) ☒ Claim(s) 34 and 35 is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 04 August 2000 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on ____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 6 and 8.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: .

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: the specification fails to include the section headings such as Back Ground of the Invention, Brief Description of the Drawings, Summary of the Invention, etc...

The abstract of the disclosure is objected to because "(Fig. 2)" should be deleted at the bottom of the Abstract. Correction is required. See MPEP § 608.01(b).

2. The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

- (a) TITLE OF THE INVENTION.
- (b) CROSS-REFERENCE TO RELATED APPLICATIONS.
- (c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
- (d) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC (See 37 CFR 1.52(e)(5) and MPEP 608.05. Computer program listings (37 CFR 1.96(c)), "Sequence Listings" (37 CFR 1.821(c)), and tables having more than 50 pages of text are permitted to be submitted on compact discs.) or
REFERENCE TO A "MICROFICHE APPENDIX" (See MPEP § 608.05(a). "Microfiche Appendices" were accepted by the Office until March 1, 2001.)
- (e) BACKGROUND OF THE INVENTION.
 - (1) Field of the Invention.
 - (2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
- (f) BRIEF SUMMARY OF THE INVENTION.
- (g) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
- (h) DETAILED DESCRIPTION OF THE INVENTION.

Art Unit: 2667

- (i) CLAIM OR CLAIMS (commencing on a separate sheet).
- (j) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
- (k) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

Drawings

3. Figure 5 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 19-33 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Meyer, R. et al (GB 2,319,128) in view of Yukutake et al (US Patent No. 5,523,713).

Hereinafter, referred to as Meyer and Yukutake.

With respect to claims 19 and 22, Meyer discloses in Fig. 6 an improved CMOS transmission gate circuit 50 comprising two cascaded transmission gates 52 and 54 with an earthing NMOS switch 56 (bypass circuit) connected to the middle node Z. Herein the switch 56 acts a mechanism to reduce injection currents in the cell and to prevent noise on the other

Art Unit: 2667

channels of the multiplexer (a bypass circuit for preventing a current flowing through the first transmission gate from reaching the other input channel, and a second transmission gate).

Further, shown in Fig. 6, the switch 56 is controlled by the select signal SEL (multiplexer circuit further comprising a control circuit for controlling the bypass channel).

Meyer does not disclose the multiplexer circuit comprising at least two input channels, an output channel, each input channel comprising a first transmission gate, which can be switched on by a select signal for connecting the input channel to the output channel.

Yukutake discloses in Fig. 12 a multiplexer circuit comprising two input channels IN1 and IN2 (multiplexer circuit comprising at least two input channels), an output channel OUT (an output channel), wherein, only a selected input is outputted according to the select signal SE (each input channel comprising a first transmission gate which can be switched on by a select signal for connecting the input channel to the output channel).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teachings of Meyer and Yukutake to include the switch 56 (bypass circuit) in the multiplexer circuit of Yukutake, to reduce injection currents in the cell and to prevent noise on other channels of the multiplexer.

With respect to claim 20, Meyer discloses in Fig. 6 that the select signal controls the switch as a function of the input voltage (control circuit controls the bypass circuit dependent upon a voltage in the input channel).

With respect to claim 21, the limitation recited in lines 1-3 “control circuit comprises a sense circuit to control said bypass circuit by sensing a voltage in the input channel” is inherent to Meyer. As shown in Fig. 6, the switch 56 is utilized to reduce the injection currents in the transmission cell when the transmission cell is closed.

With respect to claim 23, Meyer discloses in Fig. 6 that the switch 56 is active when the input channel is not selected and inactive when the input channel is selected (bypass circuit is switched on for an input channel which is not selected and is switched off for a selected input channel).

With respect to claims 24 and 30, Meyer discloses in Fig. 6 a switch 56 for reducing the injection currents into the second transmission gate 54 (bypass circuit comprising a pull-down circuit reducing an input voltage for the second transmission gate).

With respect to claim 25, Meyer discloses in Fig. 6 that the switch 56 is controlled by a select signal SEL (bypass circuit is controlled by the select signal).

With respect to claims 26 and 31, Meyer discloses in Fig. 6, a switch 56 which comprising an NMOS transistor, wherein the gate connected to the SEL, the drain connected to the output of first transmission gate, and the source connected to the ground (bypass circuit is an NMOS transistor comprising a gate, a drain, and a source, the gate of which is controlled by said

Art Unit: 2667

select signal, the drain of which is connected with an output of said first transmission gate, and the source of which is connected with ground potential).

With respect to claims 27, 28, 30, and 31, Meyer discloses (pg 8, line 36 – pg 9, line 2) that a transmission cell in accordance with the present invention formed in a P conductivity type substrate would be substantially the same as the cell 50 described above except that the with would be a PMOS transistor (pull-up circuit increasing an input voltage for the second transmission gate) having a gate electrode coupled to receive the inverse of the control signal SelN, and a second current electrode coupled to a supply voltage Vcc (pull-up circuit is a PMOS transistor comprising a drain and a source, the drain of which is connected with an output of said first transmission gate and the source of which is connected with a power supply voltage level).

With respect to claims 29 and 30, Meyer discloses in Fig. 6, the switch 56 is controlled by the select signal and the input (control circuit controls the bypass circuit by means of the select signal and an input voltage applied to the input channel).

With respect to claim 31, Meyer discloses in Fig. 2, the SELN (NAND) applied to the gate of PMOS transistor 28 and the SEL (NOR) applied to the gate of NMOS transistor 26 (control circuit comprising a NAND gate the output of which is connected with the gate of said PMOS transistor and a NOR gate the output of which is connected with gate of said NMOS transistor).

Art Unit: 2667

With respect to claim 32, Meyer discloses in Fig. 2 that the PMOS receives the input voltage and the inverter select signal and the NMOS receives the input voltage and the select signal (NAND gate receives the input voltage and the inverter select signal and NOR gate receives the input voltage and the select signal).

With respect to claim 33, Meyer discloses in Fig. 6, the switch 56 (bypass circuit) is built to prevent the flowing currents between the transmission gates (sense circuit is constructed and adapted to sense a voltage in the input channel at the input of the first transmission gate or between the first transmission gate and the second transmission gate).

With respect to claim 36, Meyer discloses in Fig. 6, the output of the CMOS transmission gate multiplexer feeds into the ADC (an ADC comprising a multiplexer circuit).

Allowable Subject Matter

5. Claims 34 and 35 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Yukutake et al (US Patent No. 5,742,551) discloses memory circuit improved in electrical characteristics.


Art Unit: 2667

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh-Vu H Ly whose telephone number is 703-306-5675. The examiner can normally be reached on Monday-Friday 7:00am - 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi Pham can be reached on 703-305-4378. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-4750.

avl


CHI PHAM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2000 02/20/03